

I claim:

1. A method for forming an interconnecting substrate, comprising  
 providing a support base,  
 disposing on said support base a decoupling capacitor, and  
 employing a deposition process to form an interconnect layer [having a  
 pattern of circuit connections] over said decoupling capacitor, whereby an  
 interconnecting substrate is formed having an embedded decoupling capacitor.
2. A method according to claim 1, including forming electrical connections on a  
 surface of said interconnect layer and extending into said interconnect layer,  
 thereby allowing devices to be mounted on said surface of said interconnect  
 layer.
3. A method according to claim 1, wherein employing a deposition process to form  
 an interconnect layer includes forming an interconnect layer having a power and  
 a ground plane.
4. A method according to claim 1, wherein employing a deposition process to form  
 an interconnect layer includes forming an interconnect layer having a plurality of  
 signal planes.
5. A method according to claim 1, wherein disposing on said support base a  
 decoupling capacitor includes disposing on said support base a plurality of  
 decoupling capacitors.

6. A method according to claim 1, wherein disposing on said support base a decoupling capacitor includes disposing on said support base a plurality of decoupling capacitors having a common ground plane.

7. A method according to claim 1, wherein disposing on said support base a decoupling capacitor includes forming a capacitor on said support base.

8. A method according to claim 1, including disposing on said support base a terminating resistor.

9. A method according to claim 1, including disposing a device on a surface of said interconnect layer at locations selected to reduce an interconnect length between said device and said decoupling capacitor.

10. A method according to claim 1, including wire bonding devices to a surface of said interconnect layer.

11. A method according to claim 1, including flip-chip mounting devices to a surface of said interconnect layer.

12. A device for interconnecting a plurality of circuit devices, comprising

a support base having a first surface,

a decoupling capacitor mounted on said first surface, and

an interconnect layer having a pattern of circuit connections and being formed over and surrounding said decoupling capacitor, whereby said decoupling capacitor is embedded within said interconnect layer.

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13. A device according to claim 12, wherein said interconnect layer includes a power plane and a ground plane, and wherein said decoupling capacitor connects in parallel between said power and ground planes.
14. A device according to claim 12, further comprising a plurality of decoupling capacitors mounted on said first surface.
15. A device according to claim 12, further comprising a resistor mounted to said first surface.
16. A device according to claim 12, wherein said support base comprises a silicon containing substrate.
17. A device according to claim 12, wherein said decoupling capacitor comprises a silicon containing dielectric material.
18. A device according to claim 12, wherein said interconnecting layer comprises a plurality of aluminum containing conductive paths.
19. A device according to claim 12 wherein said interconnecting layer comprises a plurality of copper containing conductive paths.
20. A device according to claim 12, wherein said decoupling capacitor comprises a die.

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